WHAT IS CLAIMED IS:

1. A method for programming a P-channel electrical erasable programmable read-only memory (EEPROM) having an N-well, a floating gate, a control gate, a P-type source region, a P-type drain region and a select transistor coupling the drain region to a bit line, the method comprising the steps of:

grounding the N-well;

applying a first positive voltage to the control gate;

applying a second positive voltage or a programming current to the source region; and

applying a first negative voltage to the bit line and switching on the select transistor, so that the first negative voltage is passed to the drain region, wherein

the second positive voltage or the programming current leads to a forward bias capable of turning on a parasitic bipolar transistor that includes the source region, the drain region and the N-well, and a reverse bias between the drain region and the N-well is capable of generating an electron current between the source region and the drain region for injection into the floating gate.

2. The method of claim 1, wherein the first positive voltage is 5V-6V.

3. The method of claim 1, wherein the first negative voltage is –3V- –5V.

4. The method of claim 1, wherein a second negative voltage of about –4V- –6V is applied to a gate electrode of the select transistor.

5. The method of claim 1, wherein the P-channel EEPROM is a multi-level memory cell, and the programming current is adjustable so that the multi-level memory cell can be programmed to a specific threshold voltage level.

6. A method for programming a P-channel electrical erasable programmable read-only memory (EEPROM) having an N-well, a floating gate, a control gate, a P-type source region and a P-type drain region, the method comprising the steps of:

grounding the N-well;

applying a first positive voltage to the control gate;

applying a second positive voltage or a programming current to the source region; and

applying a first negative voltage to the drain region, wherein

the second positive voltage or the programming current leads to a forward bias capable of turning on a parasitic bipolar transistor that includes the source region, the drain region and the N-well, and a reverse bias between the drain region and the N-well is capable of generating an electron current between the source region and the drain region for injection into the floating gate.

7. The method of claim 6, wherein the first positive voltage is 5V-6V.

8. The method of claim 6, wherein the first negative voltage is –3V- –5V.

9. The method of claim 6, wherein the P-channel EEPROM is a multi-level memory cell, and the programming current is adjustable so that the multi-level memory cell can be programmed to a specific threshold voltage level.